Listing of Claims:

1 – 16. (Cancelled)

17. (New) A dual processor system, comprising:

(a) a first processor having one address bus, one data bus, control signals and memory accessible via the address bus and data bus;

(b) a second processor coupled directly to the address bus, data bus and control signals of said first processor, the second processor comprising a control register with a control register system address, an internal memory, a data register having a data register system address and coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory, wherein:

the first processor can read from and write to the internal memory of the second processor by:

placing a control word on the first processor data bus and asserting the first processor address bus and control signals to select the control register of the second processor, said control word containing a starting address from which the second processor reads from or writes to said internal memory; and

the second processor, without receiving a data word count or stop address from the first processor, enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting address and incrementing upward during subsequent data transfer cycles, so long as the first processor asserts the data register system address on its address bus.

18. (New) The dual processor system of Claim 17 wherein:

in a write burst mode, following the transmission of said control word, the first processor asserts the data register system address on the first processor address bus and writes subsequent data words on the data bus, and the internal address generator selects consecutive memory locations of the internal memory, starting at the starting address, whereby the subsequent data

words are written into the consecutive memory locations until the first processor ceases to assert the data register system address; and

wherein, in a read burst mode, following the transmission of said control word, the first processor asserts the data register system address on the first processor address bus and reads subsequent data words on the data bus, the internal address generator selects consecutive memory locations of the internal memory, starting at the starting address, and the second processor clocks data words at the consecutive memory locations into the data register and places said data words on the data bus, whereby the subsequent data words are read from the consecutive memory locations by the first processor through the data register until the first processor ceases to assert the data register system address.

19. (New) The dual processor system of claim 17 wherein said control signals comprise at least a read and a write signal.

20. (New) A multi-processor system, comprising:

(a) a first processor having one address bus, one data bus, control signals and memory accessible via the address bus and data bus;

(b) at least one next processor coupled directly to the address bus, data bus and control signals of said first processor, each next processor comprising a next processor control register with a unique next processor control register system address, a next processor internal memory, a next processor data register having a unique next processor data register system address and coupled to the next processor internal memory, and a next processor internal address generator coupled to the next processor control register and to the next processor internal memory, wherein:

the first processor can read from and write to the internal memory of each next processor by:

placing a control word on the first processor data bus and asserting the first processor address bus and control signals to select the unique control register address of a

next processor, said control word containing a starting address from which the next processor reads from or writes to said next processor internal memory; and

the next processor, without receiving a data word count or stop address from the first processor, enters a burst mode in which the next processor internal address generator selects consecutive memory locations of the next processor internal memory, starting at the starting address and incrementing upward during subsequent data transfer cycles, so long as the first processor asserts the unique next processor data register system address on its address bus.

21. (New) The multi-processor system of Claim 20 wherein:

in a write burst mode, following the transmission of said control word, the first processor asserts the unique next processor data register system address on the first processor address bus and writes subsequent data words on the first processor data bus, and the next processor internal address generator selects consecutive memory locations of the next processor internal memory, starting at the starting address, whereby the subsequent data words are written into the consecutive memory locations until the first processor ceases to assert the unique next processor data register system address; and

wherein, in a read burst mode, following the transmission of said control word, the first processor asserts the unique next processor data register system address on the first processor address bus and reads subsequent data words on the data bus, the next processor internal address generator selects consecutive memory locations of the next processor internal memory, starting at the starting address, and the next processor clocks data words at the consecutive memory locations into the next processor data register and places said data words on the data bus, whereby the subsequent data words are read from the consecutive memory locations by the first processor through the next processor data register until the first processor ceases to assert the unique next processor data register system address.

22. (New) A coprocessor comprising:

a control register with a control register system address, an internal memory, a data register having a data register system address and coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory, wherein:

a master processor, having one address bus, one data bus, control signals and memory accessible via the address bus and data bus, can be coupled to said coprocessor with at least one of the signals of the address bus coupled directly to the coprocessor control register and the first processor data bus coupled directly to the coprocessor data register and to the coprocessor control register; wherein:

the master processor can read from or write to the coprocessor's internal memory in a burst mode without transmitting to the coprocessor a word count or a stop address by:

placing a control word on the master processor data bus and asserting the master processor address bus and control signals to select the control register of the coprocessor, said control word containing a starting address from which the coprocessor reads from or writes to said internal memory; and

the coprocessor, without receiving a data word count or stop address from the master processor, enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory from which the coprocessor reads from or writes to, starting at the starting address and incrementing upward during subsequent data transfer cycles, so long as the master processor asserts the data register system address on its address bus.

23. (New) The dual processor system of claim 17, wherein:

the second processor enters a single data transfer mode in which the internal address generator selects the starting internal address specified in the control word stored in the control register, and the data is transferred from the first processor to a specified location into memory of the second processor during the next data transfer cycle when the control word has a burst mode bit that does not indicate burst mode.